B2

2. (Amended) An integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively delayed from an active edge of the clock output signal by 0.5 period, 1 period, and 1.5 period of the data input signal.

Sub C1

3. (Twice Amended) An integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the data input signal.

B3

4. (Twice Amended) An integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the data input signal and by a delay time produced by a delay circuit added to the optional integer times as long as a half period of the data input signal.

REMARKS

Claims 1-18 are pending in this application, of which claims 1, 5, 9, 13, and 14 are independent. Applicants amend claims 1-4. Care has been taken to avoid the introduction of new matter. Applicants respectfully request reconsideration of the rejected claims in light of the arguments presented below.